Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claim 1 (Previously Presented): A computing system comprising:

a processor having a data/control bus interface;

a data/control bus implementing one or more device communication channels;

a mass storage device having an interface for communicating mass storage transactions;

a data memory coupled to and shared by both the processor and the mass storage device; and

a bus controller having a memory interface coupled to the data memory and a mass storage interface coupled to the mass storage device's interface without an intermediary mass storage controller and operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

Claim 2 (Original): The computing system of claim 1 wherein the data memory is coupled to the processor by a memory bus operating independent of the data/control bus.

Claim 3 (Original): The computing system of claim 2 wherein the controller comprises a memory access controller coupled to the processor, the data memory, and the mass storage device and operable to arbitrate accesses to the data memory between the mass storage and the processor.

Claim 4 (Cancelled)

Claim 5 (Original): The computing system of claim 1 wherein the data memory is coupled to the data/control bus.

Claim 6 (Cancelled)

Claim 7 (Original) The computing system of claim 1 further comprising storage controller processes and application behavior processes implemented using the processor.

Claims 8-9 (Cancelled)

Claim 10 (Original): The computing system of claim 1 wherein the processor implements data structures storing physical geometry information about the mass storage device.

Claim 11 (Cancelled)

Claim 12 (Original): The computing system of claim 1 wherein the controller is integrated with the processor on a single integrated circuit chip.

Claims 13-16 (Cancelled)

Claim 17 (Previously Presented): The computing system of claim 1 wherein the mass storage device comprises:

a spinning disk having magnetic storage media provided on at least one surface;

a head for accessing data stored in the magnetic storage media;

an actuator mechanism for moving the head relative to the magnetic storage media in response to commands;

a servo controller coupled to the data memory and configured to generate the commands to the actuator mechanism.

Claim 18 (Original): The computing system of claim 17 wherein the mass storage device's interface is implemented by the servo controller and implements a physical interface to the data/control bus and a physical interface to the head and actuator mechanism.

Claim 19 (Previously Presented): The computing system of claim 1 wherein the computing system comprises a set-top box including processes for implementing audio/video behaviors in the processor.

Claim 20 (Previously Presented): The computing system of claim 1 wherein the computing system comprises a network appliance having a network controller coupled to the data/control bus.

Claim 21 (Previously Presented): The computing system of claim 1 wherein the mass storage device comprises an optical storage device.

Claim 22 (Previously Presented): The computing system of claim 1 wherein the mass storage device comprises a magneto-optical storage device.

Claims 23-31 (Cancelled)

Claim 32 (Currently Amended): A computing system comprising:

a data/control bus implementing one or more device communication channels;

a first mass storage device having an interface for communicating mass storage transactions, wherein the mass storage device is coupled to the data/control bus;

a data memory coupled to the data/control bus;

a processor having a data/control bus interface coupled to the data/control bus, wherein the processor implements mass storage control processes to control the mass storage device;

a second mass storage device having an interface; and

a bus controller having a mass storage interface coupled to the second mass storage device's interface and operable to conduct mass storage transactions between the data memory and the second mass storage device.